CLAIMS

1-25. (Cancelled)

26. (New) An apparatus comprising:

a first supply rail;

a second supply rail;

a flip-flip having a set terminal and a reset terminal;

a regenerative latch having:

an first output terminal;

a second output terminal;

a first PMOS transistor that is coupled to the supply rail at its source, the set terminal at its drain, and the reset terminal at its gate;

a second PMOS transistor that is coupled to the supply rail at its source, the reset terminal at its drain, and the set terminal at its gate;

a first NMOS transistor that is coupled to the set terminal at its drain and the reset terminal at its gate; and

a second NMOS transistor that is coupled to the reset terminal at its drain and the set terminal at its gate; and

a clocking circuit that is coupled to the first supply rail and that gates of the first PMOS transistor, the second PMOS transistor, the first NMOS transistor, and the second NMOS transistor, wherein the clocking circuit is controlled by a clock signal;

a third NMOS transistor that is coupled to the source of the first NMOS transistor at its drain and that receives a first portion of a differential signal at its gate;

a fourth NMOS transistor that is coupled to the source of the second NMOS transistor at its drain and that receives a second portion of the differential signal at its gate;

a fifth NMOS transistor that is coupled to the sources of the third and fourth NMOS transistors at its drain and the second supply rail at its source and that receives the clock signal at its gate;

a sixth NMOS transistor that is coupled to the sources of the third and fourth NMOS transistors at its drain, the second supply rail at its source, and the first supply rail at its gate; and

a precharge circuit that is coupled to the first supply rail and the drains of the third and fourth NMOS transistors.

27. (New) The apparatus of Claim 26, wherein the clocking further comprises:

a third PMOS transistor that is coupled to the first supply rail at its source and the gate of the first PMOS transistor at it drain and that receives the clock signal at its gate;

a fourth PMOS transistor that is coupled to the first supply rail at its source and the gate of the second PMOS transistor at it drain and that receives the clock signal at its gate;

a fifth PMOS transistor that is coupled to the gates of the first and second NMOS transistors at its source and drain, respectively, and that receives the clock signal at its gate; and

a sixth PMOS transistor that is coupled to the sources of the first and second NMOS transistors at its source and drain, respectively, and that receives the clock signal at its gate.

28. (New) The apparatus of Claim 27, wherein the precharge circuit further comprises:

a seventh PMOS transistor that is coupled to the first supply rail at its source and the source of the first NMOS transistor at its drain and that receives the clock signal at its gate; and

an eighth PMOS transistor that is coupled to the first supply rail at its source and the source of the second NMOS transistor at its drain and that receives the clock signal at its gate.